Claims

1. A method for testing an integrated circuit (10) having wells (14, 18) that are wired separately from circuit VDD and ground, the method comprising the steps of:

testing a circuit including independently modifying a p-well (14) bias of an n-transistor (16) and an n-well bias (18) of a p-transistor (20); and

determining whether a defect exists from the testing.

2. The method of claim 1, wherein the wells (14, 18) include partitions, the modifying step includes applying a different well bias condition to at least one partition compared to at least one other partition, and the determining step is applied to one of the circuit as a whole and on a partition-by-partition basis.

3. The method of claim 1, wherein the wells (14, 18) include partitions, the modifying step includes applying a plurality of different well bias conditions to a plurality of different partitions, and the determining step includes comparing the results of the testing to one another to localize a defect.

4. The method of claim 1, wherein the testing step further includes stimulating the circuit with a test vector followed by the step of modifying the well biases for a predetermined time prior to the determining step.

5. The method of claim 1, wherein the determining step includes comparing outputs of the circuit to expected results for a defect-free circuit.

6. The method of claim 1, wherein the determining step includes comparing outputs of the circuit to results for the same circuit under different well bias conditions.

7. The method of claim 1, wherein the testing includes modifying the well biases to one of a plurality of extreme conditions.

8. The method of claim 6, wherein the determining step includes observing a circuit parameter in addition to well bias during the testing.

9. The method of claim 6, wherein the testing step further includes modifying at least one circuit parameter other than well bias.

10. The method of claim 1, wherein the testing step further includes voltage-based testing.

11. The method of claim 10, wherein the modifying step includes one of:

(a) decreasing a p-well (14) bias for the n-transistor (16) and decreasing an n-well

(18) bias for the p-transistor (20);

(b) increasing the p-well bias for the n-transistor and increasing the n-well bias for

the p-transistor; and

(c) increasing the p-well bias for the n-transistor and decreasing the n-well bias for

the p-transistor.

12. The method of claim 10, wherein the voltage-based testing includes applying a low-VDD.

13. The method of claim 10, wherein the modifying step includes:

first setting each well bias at a nominal value;

second increasing the p-well (14) bias of the n-transistor (16) from a nominal value and setting the n-well (18) bias of the p-transistor (20) at a nominal value; and

third setting the p-well bias of the n-transistor at a nominal value and decreasing the n-well bias of the p-transistor from a nominal value,

wherein the determining step occurs between each of the above steps.

14. The method of claim 13, wherein the modifying step further includes:

fourth setting the p-well (14) bias of the n-transistor (16) to a lower than nominal value and the n-well (18) bias of the p-transistor (20) to a higher than nominal value;

fifth setting the p-well bias of the n-transistor to a lower than nominal value and

the n-well bias of the p-transistor to a lower than nominal value;

sixth setting the p-well bias of the n-transistor to a higher than nominal

value and the n-well bias of the p-transistor to a higher than nominal value,

wherein the determining step occurs between each of the above steps.

15. The method of claim 10, wherein the determining step includes determining at least one of a minimum well bias and a maximum well bias at which the IC (10) functions at a particular speed; and determining whether at least one minimum and maximum well bias meets a predetermined goal.

16. The method of claim 1, wherein the testing includes measuring an elevated static leakage current (IDDQ).

17. The method of claim 16, wherein the modifying step includes applying both increases and decreases of well bias to establish a relationship between IDDQ and well bias.

18. The method of claim 16, wherein the step of applying includes:

applying a first set of biases to the n-well (18) and the p-well (14), and then measuring IDDQ; and

applying a different second set of biases to the n-well and the p-well, and then measuring IDDQ.

19. The method of claim 16, wherein the determining step includes comparing the results of the applying step to expected results for a defect-free circuit.

20. The method of claim 16, wherein the determining step includes:

establishing an IDDQ curve shape for a defect-free circuit from the applying steps;

establishing an IDDQ curve shape for a circuit under test; and

comparing the curve shapes.

21. The method of claim 16, wherein the modifying step includes setting a well bias to at least substantially decrease one type of IDDQ, and the step of determining includes performing a characterization of the other type of IDDQ versus at least one circuit parameter.

22. The method of claim 1, wherein the testing includes stress testing.

23. The method of claim 22, wherein the modifying step includes modifying well bias to modify switching current.

24. The method of claim 22, wherein the modifying step includes modifying well bias to modify current during at least one of burn-in stressing and high-voltage stressing.

25. The method of claim 22, wherein the modifying step includes modifying well bias to draw a predetermined amount of at least one of switching and static current.

26. The method of claim 22, wherein the modifying step includes:

increasing the p-well bias and decreasing the n-well bias when circuit switching is to occur; and

decreasing the p-well bias and increasing the n-well bias when circuit switching is

not to occur.

27. The method of claim 22, wherein the modifying step includes setting well-bias at a first setting during high voltage burn-in and a second setting during nominal voltage burn-in.

28. The method of claim 22, wherein the modifying step includes setting well-bias during burn-in to maintain circuit functioning.

29. The method of claim 22, wherein the modifying step includes setting well-bias to maintain a stress test temperature.

30. The method of claim 22, wherein the modifying step includes modifying well bias during stressing to accelerate defects by placing an elevated electric field across a gate oxide of the circuit.

31. A method for testing a semiconductor circuit (10) having wells (14, 18) that are wired separately from circuit VDD and ground, the method comprising the steps of:

testing the circuit for a defect by measuring static leakage current; and

increasing and decreasing well biases of an n-transistor (16) and a p-transistor (20) to change respective transistor threshold voltages during testing.

32. A system for testing a semiconductor circuit (10) having wells (14, 18) that are wired separately from circuit VDD and ground, the system comprising:

means for testing (60) the circuit including independently modifying a well bias of

an n-transistor (16) and a well bias of a p-transistor (20); and

means for determining (62) whether a defect exists from the testing.

33. The system of claim 32, further comprising a temperature sensor (50, 52) for monitoring a temperature of the IC, wherein the means for testing (60) modifies the well biases to maintain a stress test temperature.